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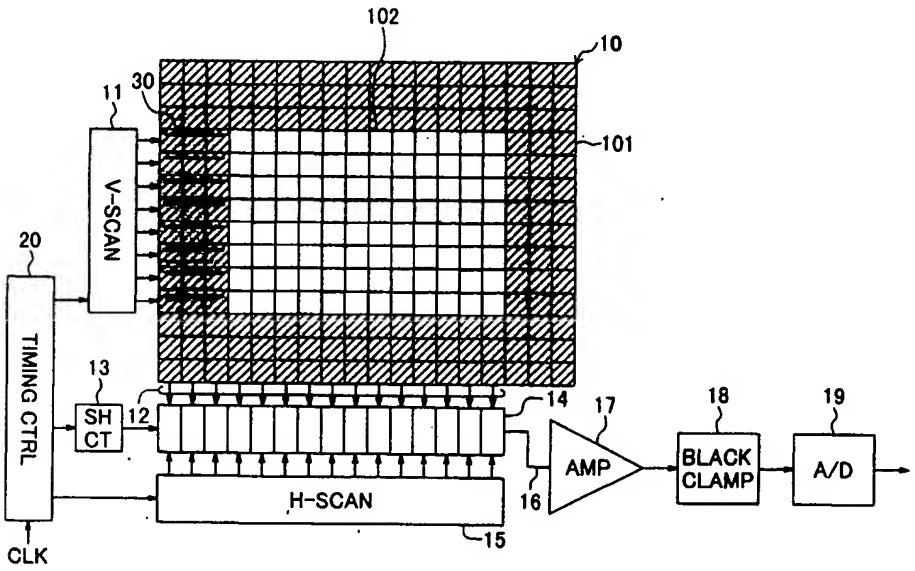
## (54) Image sensor with black level control and low power consumption

(57) An image sensor comprising a pixel array (10), comprising at least one row of pixels, each pixel having a light receiving element and a reset switch (41-45) connected to a reset node of said light receiving element, divided into an effective pixel region (102) and an optical black pixel region (10); and a read-out circuit, for scanning said pixel array (10) to read out signals from said pixels, including a black clamp circuit for holding a signal from said optical black pixel region (101) as an integrated dark current signal and for correcting a signal from said effective pixel region (102) with said integrated dark current signal, wherein said optical black pixel region comprises a potential averaging line (30) commonly connected to said reset nodes of a plurality of pixels in a pixel row.

*FIG.1*

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## Description

**[0001]** The present invention relates generally to an image sensor, and more particularly, to an image sensor having a plurality of pixels arranged in rows and columns, for use, for example, in an electronic camera, an image reader or a facsimile apparatus, with a stabilized black level and low power consumption.

**[0002]** In an image sensor, each light receiving element outputs a signal having an integrated light component and an integrated dark current component. This dark current has such a strong temperature dependency that the current is approximately doubled with a rise of 9°C.

**[0003]** In order to remove the integrated dark current component from the signal to obtain a true integrated light signal, in the prior art, the peripheral region of a pixel array is covered with a light shielding film to form an optical black pixel region, and an integrated dark current signal is read out from the optical black pixels in a blanking period to obtain an average voltage Vd of the integrated dark current signals in a black clamp circuit as an offset value (a black clamp level). The average voltage Vd is subtracted from each pixel signal Vs in the black clamp circuit during a period when an effective pixel region is read.

**[0004]** Two methods of performing black clamps may be adopted by the black clamp circuit, one is a line black clamp method performed in horizontal scanning, and the other is a frame black clamp method performed in each frame.

**[0005]** FIG. 19 shows an integrated dark current signal read out from an optical black pixel region in a horizontal blanking period. The signal is not constant according to characteristics of each pixel.

**[0006]** When a defective pixel exists, an integrated dark current signal suddenly changes as shown in FIG. 19, therefore, an offset value becomes incorrect in a black clamp circuit having an integration capacitor for obtaining an average value, which causes lateral stripe noise. If the width of the optical black pixel region is made wide in order to prevent the noise, the offset component cannot be obtained in a horizontal blanking period in an image sensor having many pixels, and IC size is increased which results in increased cost.

**[0007]** In an image sensor adopted in portable equipment, a reduction in power consumption is required.

**[0008]** The following methods are used for reduction in power consumption of a semiconductor chip:

(1) stopping an operation clock in a period where no operation is required; and
(2) reducing a clock frequency by dividing it, for example, by a half, a quarter or one-eighth.

**[0009]** An image sensor chip includes an analogue circuit and a digital circuit, where the power consumption of the analog circuit is larger than that of the digital circuit by a large ratio, and therefore the power consumption of an image sensor used for taking a moving picture cannot be decreased to a great extent by such methods.

**[0010]** When a power source for the analog circuit is on/off controlled, the effect of the off period only appears after one frame, and therefore the power source cannot be simply turned off.

**[0011]** Accordingly, it is a consideration of the present invention to provide an image sensor capable of preventing variations in black level due to a pixel defect.

**[0012]** It is another consideration of the present invention to provide an image sensor capable of obtaining a black clamp level in a shorter time.

**[0013]** It is still another consideration of the present invention to provide an image sensor capable of decreasing power consumption by performing fine on/off control of a power source for an internal circuit in a case of a reduced frame rate.

**[0014]** Aspects of the invention are as defined in the accompanying independent claims.

**[0015]** In one of the aspects of the present invention, an image sensor comprises a potential averaging line commonly connected to reset nodes of a plurality of pixels in a pixel row in an optical black pixel region.

**[0016]** With this aspect, a potential averaging process is automatically performed before reading out a signal from the optical black pixel region instead of performing an averaging process in a black clamp circuit as in the prior art. Therefore, a black level (integrated dark current signal) is stabilized, a more accurate line black clamp is performed, and lateral stripe noise is reduced, thereby improving the image quality.

**[0017]** Further, since an integrated dark current signal needs only to be sampled at a specific time, the configuration of a black clamp circuit is made simpler than that of the prior art.

**[0018]** Furthermore, since a black clamp level (an offset value) is obtained in a shorter time than in the prior art because of the above described reason, there is no problem even if many pixels exist in a pixel array and thereby a blanking period is short.

**[0019]** In another of the aspects of the present invention, there is provided an image sensor comprising a control circuit for repeating sequential operation of a light integration period, a read-out period and a power-off period, wherein the control circuit: in the light integration period, causes a pixel array to perform light integration without supplying power to a read-out circuit; in the read-out period, causes the read-out circuit to read out integrated signals; and in the power-off period, ceases to supply power to the pixel array and the read-out circuit.

**[0020]** With this aspect, power supply for the read-out circuit ceases in the light integration period, and the power supply to the pixel array and the read-out circuit ceases in the power-off period, thereby reducing power consumption in the image sensor.

[0021] A detailed description will now be given, by way of example, with reference to the accompanying drawings, in which:

FIG. 1 is a schematic block diagram showing a first embodiment of an image sensor according to the present invention;
FIG. 2 is a circuit diagram of part of a pixel array shown in FIG. 1;
FIG. 3 is a graph showing an integrated dark current signal (voltage) read out from an optical black pixel region in a horizontal blanking period;
FIG. 4 is a schematic block diagram showing a second embodiment of an image sensor according to the present invention;
FIG. 5 is a schematic block diagram showing a third embodiment of an image sensor according to the present invention;
FIG. 6 is a schematic block diagram showing a fourth embodiment of an image sensor according to the present invention;
FIG. 7 is a circuit diagram showing a potential averaging line 30A of FIG. 6 and part of its peripheral circuitry;
FIG. 8 is a schematic block diagram showing a fifth embodiment of an image sensor according to the present invention;
FIG. 9 is a circuit diagram showing potential averaging lines 30A to 30D of FIG. 8 and part of their peripheral circuitry;
FIG. 10 is a schematic block diagram showing a sixth embodiment of an image sensor according to the present invention;
FIG. 11 is a schematic block diagram showing a seventh embodiment of an image sensor according to the present invention;
FIG. 12 is a time chart showing operation of a power source control circuit shown in FIG. 11;
FIG. 13 is a schematic block diagram showing an eighth embodiment of an image sensor according to the present invention;
FIG. 14 is a time chart showing operation of a power source control circuit shown in FIG. 13;
FIG. 15 is a schematic block diagram showing a ninth embodiment of an image sensor according to the present invention;
FIG. 16 is a time chart showing operation of a power source control circuit shown in FIG. 15;
FIG. 17 is a schematic block diagram showing a tenth embodiment of an image sensor according to the present invention;
FIG. 18 is a time chart showing operation of a power source control circuit shown in FIG. 16; and
FIG. 19 is a graph showing an integrated dark current signal read out from a prior art optical black pixel region in a horizontal blanking period.

[0022] Like reference characters designate like or corresponding parts throughout the drawings.

First Embodiment

[0023] FIG. 1 is a schematic block diagram showing a first embodiment of an image sensor according to the present invention.

[0024] The image sensor is, for example, of a MOS type.

[0025] A pixel array 10 has pixels arranged in rows and columns. A hatched peripheral portion in the pixel array 10 is an optical black pixel region 101 in which light receiving elements are covered with a light shielding film such as an aluminum film. Since light cannot enter into the light receiving elements in the optical black pixel region 101, only an integrated dark current signal is read out from this region. An area inside the optical black pixel region 101 is an effective pixel region 102 with no light shielding film thereon.

[0026] In a horizontal scanning start side of the optical black pixel region 101 and beneath the light shielding film, potential averaging lines 30 (drawn with thick lines in FIG. 1) are formed along pixel rows.

[0027] Pixels of the optical black pixel region 101 are the same as those of the effective pixel region 102 with only the exception that the light shielding film is formed above the pixels of the optical black pixel region 101 and the potential averaging lines 30 are formed in some of the pixels of the optical black pixel region.

[0028] FIG. 2 is a circuit diagram of part of a pixel array 10 of FIG. 1.

[0029] In an optical black pixel 1021, the anode of a photodiode 31 as a light receiving element is connected to ground, while the cathode of the photodiode 31 is connected, on one hand, through a buffer amplifier 32 and a read-out switch element 33 to a vertical bus line 121 and, on the other hand, through a reset switch element 41 to a reset potential supply line 40. The buffer amplifier 32 is, for example, a source follower circuit. The read-out switch element 33 and the reset switch 41 are each constituted by a FET. Reset switch elements 42 to 45 are provided in respective pixels 1022 to 1025. The reset switch elements 42 to 45 are connected between the cathodes of photodiodes and the reset potential supply line 40.

[0030] The control inputs of the read-out switch elements on the same row are commonly connected to a row select line 50 which is a gate line, and the control inputs of the reset switch elements 41 to 45 are commonly connected to a row reset line 51 which is a gate line. To the row select line 50 and the row reset line 51, a row select signal RS1 and a reset signal RST1, respectively, are provided from a vertical scanning circuit 11 of FIG. 1. The reset ends (cathodes) of the photodiodes of the optical black pixels 1021 to 1023 are commonly connected to the potential averaging line 30 (drawn with a thick line).

[0031] A read-out switch element 33 is turned on by

a pulse of the row select signal RS1 and thereby the cathode potential of the photodiode 31 is read out through the buffer amplifier 32 and the read-out switch element 33 onto the vertical bus line 121. Similarly, in regard to the pixels 1022 to 1025, the cathode potentials of the photodiodes are read out through buffer amplifiers and read-out switch elements onto vertical bus lines 122 to 126, respectively. Then, the reset switches 41 to 45 are turned on by a pulse of the reset signal RST1 and the cathode potentials of the photodiodes are reset to VDD.

**[0032]** Operations for reading out and resetting the pixels 1021 to 1025 are performed every frame period. In one frame period from a reset to the next reset, electric charges accumulated in the photodiodes of the effective pixels 1024 and 1025 are discharged by incident light and dark current, while the electric charges in the optical black pixels 1021 to 1023 are discharged only by dark current.

**[0033]** Referring back to FIG. 1, the vertical scanning circuit 11 including a shift register sequentially activates row select lines on the pixel array 10. Thereby, signals integrated on light receiving elements on a selected row are read out onto a vertical bus 12 (vertical read out). The read-out signals are held in respective sample and hold circuits 14 in response to activation of a control signal from a sample and hold control circuit 13. The light receiving elements on the selected row are reset as described above to start integration again.

**[0034]** The sample and hold circuits 14 are, for example, correlation double sampling circuits (CDS) and in this case, the sampling and holding of each integrated signal will be described as follows. Firstly, the sample and hold circuits 14 are reset. Then a voltage ((an integrated signal Vx) + (a component DV depending on the variations in characteristics of the buffer amplifier 32 and the read-out switch element 33 coupled to the photodiode 31)) is sampled corresponding to one of the sample and hold circuits 14. Next a pixel on a selected row is reset. Thereafter, a second sampling is performed to hold the difference Vx = (Vx + DV) - DV in a corresponding one of the sample and hold circuits 14.

**[0035]** A horizontal scanning circuit 15 including a shift register sequentially activates the sample and hold circuits 14 from left to right in FIG. 1 to read out signals therefrom onto a horizontal bus 16. The signal on the horizontal bus 16 is amplified by an amplifier circuit 17.

**[0036]** The integrated dark current signal is read out onto the horizontal bus 16 during each horizontal blanking period and the voltage thereof is constant as shown in FIG. 3. That is, since the voltage has been averaged, prior to read out, by the potential averaging line 30, no averaging in black clamp circuit 18 is required. The black clamp circuit 18 samples the voltage, for example, at a time t1 shown in FIG. 3 and holds the sampled voltage as a black clamp level Vb. When reading out an integrated signal from an effective pixel, the black clamp circuit 18 subtracts the black clamp voltage Vb from the integrated voltage signal Vs on the horizontal bus 16. Such a black level correcting operation is performed on each horizontal line and is called a line black clamp.

**[0037]** The black level corrected signal is converted to a digital value by an A/D converter circuit 19.

**[0038]** A timing control circuit 20 generates control signals for operating the vertical scanning circuit 11, the sample and hold circuit 13 and the horizontal scanning circuit 15 based on a clock signal CLK.

**[0039]** Referring back to FIG. 2, in the optical black pixels 1021 to 1023, since the reset ends of the photodiodes are commonly connected to the potential averaging line 30, the integrated dark current signals read out from the vertical bus lines 121 to 123 are almost equal to one another. Differences among the integrated dark current signals on the optical black pixels 1021 to 1023 caused by variations in characteristics of the buffer amplifiers 32 and the read-out switch elements 33 are removed through the above described operation of the sample and hold circuits 14.

**[0040]** In the first embodiment, since a reset node in each pixel on the same row in the optical black pixel region 101 is commonly connected to the potential averaging line 30, a potential averaging process is automatically performed prior to a signal read out from the optical black pixel region 101 instead of an averaging process performed in the black clamp circuit 18 in the prior art, thereby stabilizing a read-out signal level. Hence, a more accurate line black clamp is realized, thereby reducing lateral stripe noise to improve image quality.

**[0041]** Further, since the integrated dark current signal has only to be sampled at a specific time, the construction of the black clamp circuit 18 can be more simplified than that of the prior art.

Second Embodiment

**[0042]** FIG. 4 is a schematic block diagram showing a second embodiment of an image sensor according to the present invention.

**[0043]** In this embodiment, among the vertical bus lines in the optical black pixel region 101, only the vertical line 123 of FIG. 2 is connected to a signal input of one of a plurality of sample and hold circuits 14A.

**[0044]** Thereby, even when the number of pixels in the pixel array 10 is large and in turn the horizontal blanking period is short, the black clamp level can be correctly sampled by the black clamp circuit 18 in this short period.

**[0045]** Further, the number of the sample and hold circuits 14A and stages of horizontal scanning circuits 15A can be smaller than that in the case of FIG. 1.

**[0046]** Since other points in this embodiment are the same as those of the first embodiment, further description of this embodiment has been omitted.

Third Embodiment

**[0047]** FIG. 5 is a schematic block diagram showing a third embodiment of an image sensor according to the present invention.

**[0048]** In this embodiment, a mode signal MODE is provided to a horizontal scanning circuit 15B. The circuit 15B scans from the left side to the right side in FIG. 5 when the mode signal MODE indicates a normal image mode, and scans in the opposite direction when the mode signal MODE indicates a left/right reverse image mode (or a top/bottom and left/right reverse image mode).

**[0049]** It is necessary to determine the black clamp level for each horizontal line prior to scanning effective pixels on the same line, so potential averaging lines (drawn with thick lines) are formed on both sides of horizontal scanning lines. One vertical bus line is connected to a signal input of the end one of a plurality of sample and hold circuits 14B, at both sides of the horizontal scanning lines.

**[0050]** Since other points in this embodiment are the same as those of the second embodiment, further description of this embodiment has been omitted.

Fourth Embodiment

**[0051]** FIG. 6 is a schematic block diagram showing a fourth embodiment of an image sensor according to the present invention.

**[0052]** In this embodiment, in order to perform a frame black clamp, potential averaging lines 30A to 30C are provided on respective pixel rows on the vertical scanning start side in the optical black pixel region 101.

**[0053]** The number of sample and hold circuits 14C and stages of a horizontal scanning circuit 15C is equal to the number of columns of the effective pixel region 102 and smaller than in the case of FIG. 4 by 1. Further, the number of stages of a vertical scanning circuit 11A is larger than the number of rows of the effective pixel region 102 by the number of potential averaging lines.

**[0054]** FIG. 7 is a circuit diagram showing the potential averaging line 30A of FIG. 6 and part of the peripheral circuitry thereof.

**[0055]** In FIG. 6, the black clamp circuit 18 has an integration circuit for obtaining an average of voltages read out from potential averaging lines 30A to 30C each through a buffer amplifier, a read-out switch and a vertical bus line. The black clamp circuit 18 holds the average as the black clamp level Vb and thereafter outputs an integrated light signal by subtracting the black clamp level Vb from the effective pixels' integrated signal Vs on the horizontal bus 16. Such a black pixel correcting operation is performed every frame and is called a frame black clamp.

**[0056]** In the fourth embodiment, a similar effect as that of the first embodiment is obtained.

Fifth Embodiment

**[0057]** FIG. 8 is a schematic block diagram showing a fifth embodiment of an image sensor according to the present invention.

**[0058]** In this embodiment, potential averaging lines 30A to 30C are connected to each other through a common line 30D.

**[0059]** FIG. 9 shows potential averaging lines 30A to 30D of FIG. 8 and part of the peripheral circuitry thereof.

**[0060]** The potential averaging lines 30A to 30D also function as the reset potential supply line 40 of FIG. 2. That is, the reset switch element 41 commonly used for three pixel rows is connected to the common line 30D. Since an integrated dark current signal in common with the three pixel rows can be read out from each vertical bus line, row select lines 50A, 50B and 50C for the three pixel rows are also commonly connected to each other through a common line 50D, and a row select signal RS0 is provided to the common line 50D to commonly turn on/off read-out switch elements for the three pixel rows.

**[0061]** Since only the row select signal RS0 is sufficient for the three pixel rows, the number of stages of the vertical scanning circuit 11B is one more than the number of rows in the effective pixel region 102, and the configuration thereof is thus simpler than that of the vertical scanning circuit 11A of FIG. 6.

**[0062]** Further, since the black clamp period in the vertical blanking period can be 1/3 of that in the case of the fourth embodiment, the fifth embodiment is especially advantageous in a case where the number of pixels of the pixel array 10 is large and therefore the vertical blanking period is short.

**[0063]** Since other points in this embodiment are the same as those of the fourth embodiment, further description of this embodiment has been omitted.

Sixth Embodiment

**[0064]** FIG. 10 is a schematic block diagram showing a sixth embodiment of an image sensor according to the present invention.

**[0065]** In this embodiment, the mode signal MODE is provided to a vertical scanning circuit 11D which scans from the top side to the bottom side in FIG. 10 when the mode signal MODE indicates a normal image mode, and scans in the opposite direction when the mode signal MODE indicates a top/bottom reverse image mode (or a top/bottom and left/right reverse image mode).

**[0066]** Since it is necessary to determine the black clamp level for each horizontal line prior to scanning effective pixels in the same frame, potential averaging lines (drawn with thick lines) are formed on both sides of the vertical scanning lines.

**[0067]** On both sides of the vertical scanning lines, one row select signal (commonly used for a plurality of rows) is connected to the output of the vertical scanning circuit 11D.

**[0068]** Since other points of this embodiment are the same as those of the fifth embodiment, further description of this embodiment has been omitted.

Seventh Embodiment

**[0069]** FIG. 11 is a schematic block diagram showing a seventh embodiment of an image sensor according to the present invention.

**[0070]** A reference voltage generating circuit 21a supplies a reset voltage to the pixel array 10 and reference voltages to the sample and hold circuits 14 and the amplifier circuit 17. The reference voltage generating circuit 21a is a constituent of a power source circuit 21.

**[0071]** The mode signal MODE is provided to the power source circuit 21, and the power source circuit 21 supplies power source voltages to circuits at all times when the mode signal indicates a normal mode. The power source circuit 21 supplies the power source voltage to a block BL1 when an enable signal EN1 from a power source control circuit 22 is active and ceases the supply when the signal EN1 is inactive, while supplying the power source voltages to a block BL2 when an enable signal EN2 from the power source control circuit 22 is active and ceasing the supply when the signal EN2 is inactive.

**[0072]** The block BL1 includes the pixel array 10 and the vertical scanning circuit 11. The block BL2 includes the sample and hold control circuit 13, the sample and hold circuits 14, the horizontal scanning circuit 15, the amplifier circuit 17 and the A/D converter circuit 19. Although the block BL2 includes the black clamp circuit as well, its description is omitted here for simplification, and this also applies in the other embodiments mentioned below.

**[0073]** The power source circuit 21 supplies a power source voltage to the timing control circuit 20 and the power source control circuit 22 at all times even in a low power consumption mode.

**[0074]** Since the reference voltage generating circuit 21a is a constituent of the power source circuit 21, the reference voltage generating circuit 21a supplies the reset voltage to the pixel array 10 when the power source circuit 21 supplies the power source voltage to the block BL1, while the reference voltage generating circuit 21a supplies the reference voltages to the sample and hold circuits 14 and the amplifier circuit 17 when the power source circuit 21 supplies the power source voltage to the block BL2.

**[0075]** In the power source control circuit 22, a vertical sync signal VSYNC from the timing control circuit 20 is provided to the clock input of a counter 23, the lowest bit Q0 of the counter provides the enable signal EN2 and the highest bit Q1 of the counter 23 is provided to an inverter 24 to generate the enable signal EN1. The counter 23 outputs counts 0, 1 and 2 cyclically and the enable signal EM1 is high when the count is 0 or 1, while the enable signal EN2 is high when the count is 1.

**[0076]** FIG. 12 is a time chart showing operation of the power source control circuit 22 of FIG. 11.

**[0077]** Next, a description will be given of operation of the embodiment configured as described above in a case of a low power consumption mode.

**[0078]** In an initial state, assume that the count of the counter 23 is 2. In this state, the power source voltages are supplied to neither of the blocks BL1 and BL2.

(Light integration period)

**[0079]** In response to the rising edge of the vertical sync signal VSYNC, the count of the counter 23 becomes 0 and the enable signal EN1 goes high and the power source voltage is supplied to the block BL1.

**[0080]** The pixel lines are sequentially activated by the vertical scanning circuit 11 in response to the control signal from the timing control circuit 20. That is, the above described vertical read out and resetting are sequentially performed line by line. Since the power source voltages are not supplied to the block BL2, no power consumption thereof arises.

(Reading-out period)

**[0081]** In response to the rising edge of the vertical sync signal VSYNC, the count of the counter 23 becomes 1 and the enable signal EN2 goes high and the power source voltages are also supplied to the block BL2.

**[0082]** In the block BL1, the pixel lines are sequentially activated and the vertical read out and resetting are performed line by line. In the block BL2, the horizontal read out is performed after each time pixel signals from a selected row are latched in the sample and hold circuits 14.

**[0083]** That is, the operation of the read out period is the same as that of the normal mode.

(Power-off period)

**[0084]** In response to the rising edge of the vertical sync signal VSYNC, the count of the counter 23 becomes 2 and the enable signals EN1 and EN2 go low to cease the supply of the power source voltages to the blocks BL1 and BL2.

**[0085]** The light integration, the read out and the power-off periods described above are cyclically repeated.

**[0086]** Currents used in various sections of the image sensor are, for example, as follows:

about 1 mA into the pixel array 10,
about 3 mA in total to the vertical scanning circuit 11, the sample and hold control circuits 13, the horizontal scanning circuit 15, the timing control circuit 20 and the power source control circuit 22,
about 2.5 mA into the sample and hold circuits 14,
about 8 mA into the amplifier circuit 17,

about 12 mA into the A/D converter circuit 19,
about 0.5 mA into the reference voltage generating circuit 21a, and
about 22.5 mA in total to the sample and hold circuits 14, the amplifier circuit 17 and the A/D converter circuit 19 in the block BL2, wherein this current is comparatively large.

**[0087]** According to this seventh embodiment, the power supply to the block BL2 ceases in the light integration period and moreover, the power supply to the blocks BL1 and BL2 ceases in the power-off period, therefore, in a 10 frame period for example, the power consumption of the image sensor can be reduced to about 1/3 of that in the normal mode.

Eighth Embodiment

**[0088]** FIG. 13 is a schematic block diagram showing an eighth embodiment of an image sensor according to the present invention.

**[0089]** A power source circuit 21A supplies its power source voltage to the pixel array 10 at all times even in the low power consumption mode.

**[0090]** In the low power consumption mode, the power source circuit 21A supplies the power source voltage to the vertical scanning circuit 11 when an enable signal EN1A is active, while ceasing the supply when the enable signal EN1A is inactive.

**[0091]** In a power source control circuit 22A, the output bit Q0 of the counter 23 is provided to the inverter 24 to generate the enable signal EN1A and the output bit Q1 of the counter 23 provides an enable signal EN2.

**[0092]** The other constituents of this embodiment are the same as those of FIG. 11.

**[0093]** FIG. 14 is a time chart showing the operation of the power source control circuit 22A of FIG. 13.

**[0094]** Next, a description will be given of the operation of the image sensor configured as described above in a case of the low power consumption mode.

**[0095]** In an initial state, assume that the count of the counter 23 is 2. In this state, the power source voltages are supplied to the vertical scanning circuit 11 and the block BL2.

(First light integration period)

**[0096]** In response to the rising edge of the vertical sync signal VSYNC, the count of the counter 23 becomes 0, the enable signal EN2 goes low and supply of the power source voltage to the block BL2 ceases.

**[0097]** The vertical scanning circuit 11 performs vertical scanning in response to the control signal from the timing control circuit 20. Thereby, the above described read out and resetting are performed line by line.

(Second light integration period)

**[0098]** In response to the rising edge of the vertical sync signal VSYNC, the count of the counter 23 becomes 1 and the enable signal EN1A goes low and supply of the power source voltage to the vertical scanning circuit 11 ceases.

**[0099]** Thereby, only the light integration is performed in the pixel array 10.

(Reading-out period)

**[0100]** In response to the rising edge of the vertical sync signal VSYNC, the count of the counter 23 becomes 2, the enable signals EN1 and EN2 go high and the power source voltages are supplied to the blocks BL1 and BL2.

**[0101]** Thereby, the same operation as read out in the seventh embodiment is performed.

**[0102]** The periods of first and second light integration and reading-out described above are cyclically repeated.

**[0103]** According to this eighth embodiment, supply of the power source voltage to the block BL2 is cut off in the first and second light integration periods and the state is similar to the power-off state. Therefore, in 15 frame periods for example, power consumption of the image sensor can be reduced to a value lower than 5.0% of that in the normal operation mode. Further, light integration periods are twice as long as in the first embodiment to improve the sensitivity of the image sensor.

**[0104]** Note that the second light integration period may be a plurality of frames to increase the length of the light integration period by replacing the counter 23 of the power source control circuit 22A with a scale-of-N counter, where $N > 3$, and changing the logic circuit configuration.

Ninth embodiment

**[0105]** FIG. 15 is a schematic block diagram showing a ninth embodiment of an image sensor according to the present invention.

**[0106]** A power source circuit 21B supplies the power source voltage to the pixel array 10 and the vertical scanning circuit 11 at all times even in the low power consumption mode. Therefore, there is no need to provide the enable signal EN1 to the power source circuit 21B.

**[0107]** In a power source control circuit 22B, the output bits Q0 and Q1 of the counter 23 are provided to an OR gate 25 to generate the enable signal EN2.

**[0108]** The other constituents of this embodiment are the same as those of FIG. 11.

**[0109]** FIG. 16 is a time chart showing the operation of the power source control circuit 22B of FIG. 15.

**[0110]** Next, a description will be given of operation of the embodiment configured as described above in the

case of the low power consumption mode.

**[0111]** In an initial state, assume that the count of the counter 23 is 2. In this state, the power source voltage is supplied to the block BL2.

(Light integration period)

**[0112]** In response to the rising edge of the vertical sync signal VSYNC, the count of the counter 23 becomes 0 and the enable signal EN2 goes low and supply of the power source voltage to the block BL2 ceases.

**[0113]** The vertical scanning circuit 11 performs vertical scanning in response to the control signal from the timing control circuit 20. Thereby, the above-described vertical read out and resetting are performed line by line.

(First read out period)

**[0114]** In response to the rising edge of the vertical sync signal VSYNC, the count of the counter 23 becomes 1 and the enable signal EN2 goes high and the power source voltages are supplied to the block BL2.

**[0115]** Thereby, the same operation as the read out in the seventh embodiment is performed.

(Second read out period)

**[0116]** The count of the counter 23 becomes 2 in response to the rising edge of the vertical sync signal VSYNC and the enable signal EN2 remains high.

**[0117]** Thereby, the same operation as the read out described above is performed.

**[0118]** Such light integration, first read out and second read out periods are cyclically repeated.

**[0119]** According to this ninth embodiment, since the supply of the power source voltages to the block BL2 are cut off in the light integration period, the state is similar to the power-off state and power consumption of the image sensor can be reduced to about 2/3 of that in the normal operation mode. Moreover, since read out is performed in two of three frames, a frame rate can be increased to twice that in the seventh embodiment.

Tenth Embodiment

**[0120]** FIG. 17 is a schematic block diagram showing a tenth embodiment of an image sensor according to the present invention.

**[0121]** This image sensor is analogous to that of FIG. 11 but differs from the seventh embodiment in that the enable signal EN2 of FIG. 11 is divided into enable signals EN21 to EN23.

**[0122]** In the low power consumption mode, a power source circuit 21C supplies the power source voltages as follows: the enable signal EN21 is active in the sample and hold control circuit 13, the sample and hold circuits 14 and the horizontal scanning circuit 15, the enable signal EN22 is active in the amplifier circuit 17, and the enable signal 23 is active to the A/D converter circuit 19.

**[0123]** In a power control circuit 22C, a logic circuit 26 generates the enable signals EN21 to EN23 shown in FIG. 18 according to the output bit Q0 of the counter 23 and timing correction signals from the timing control circuit 20. The rising and falling edges of the enable signals EN21 to EN23 are thus made to deviate a little from one another.

**[0124]** The other constituents of this embodiment are the same as those of FIG. 11.

**[0125]** Description of the operation of the above-described configuration is omitted since it is apparent from the description of the seventh embodiment and FIG. 18.

**[0126]** According to this tenth embodiment, since a sudden change in current is reduced due to the deviations of the rising and falling edges of the enable signals EN21 to EN23, variations in the power source voltage are smaller than in the seventh embodiment.

**[0127]** Although preferred embodiments of the present invention have been described, it is to be understood that the invention is not limited thereto and that various changes and modifications may be made without departing from the scope of the invention.

**[0128]** For example, in the first to tenth embodiments, the image sensor may be of a one-dimensional type.

**[0129]** In the seventh embodiment, the power-off period may be two vertical scanning periods or longer if a further reduced frame rate is not a problem.

**[0130]** Further, the A/D converter circuit 19 need not be a constituent of the image sensor. Instead of the amplifier circuit 17 connected to the horizontal bus 16, amplifier circuits connected to respective vertical bus lines may be employed. The image sensor is not limited to the MOS type but may be a CCD type.

## Claims

1. An image sensor comprising:

a pixel array, comprising at least one row of pixels, each pixel having a light receiving element and a reset switch connected to a reset node of said light receiving element, divided into an effective pixel region and an optical black pixel region; and

a read-out circuit, for scanning said pixel array to read out signals from said pixels, including a black clamp circuit for holding a signal from said optical black pixel region as an integrated dark current signal and for correcting a signal from said effective pixel region with said integrated dark current signal,

wherein said optical black pixel region comprises a potential averaging line commonly connected to said reset nodes of a plurality of pixels in a pixel row.

2. The image sensor of claim 1, wherein pixels including said potential averaging line are located outside of said effective pixel region in a horizontal scanning direction, and a line clamp is performed by said black clamp circuit.

3. The image sensor of claim 1, wherein said pixel array comprises a plurality of pixels arranged in rows and columns, pixels including said potential averaging line are located outside of said effective pixel region in a vertical scanning direction, and a frame clamp is performed by said black clamp circuit.

4. The image sensor of claim 3, wherein said potential averaging lines in a plurality of pixel rows are connected to each other, and said reset switch is commonly connected to said potential averaging lines.

5. The image sensor of claim 1 or 2, wherein said pixel array comprises a plurality of pixels arranged in rows and columns, and each column comprises a vertical bus line coupled to pixels of this column in order to read out a signal from a pixel of a selected row,

wherein said read-out circuit further comprises a correlation double sampling circuit for each column, and said correlation double sampling circuit is coupled between said vertical bus line of this column and said black clamp circuit.

6. An image sensor comprising:

a pixel array, comprising a plurality of pixels, each pixel having a light receiving element;
a read-out circuit, for scanning said pixel array to read out signals from pixels; and
a control circuit, arranged to repeat a sequential operation of a light integration period, a read-out period and a power-off period,
wherein said control circuit:

in said light integration period, causes said pixel array to perform light integration without supplying power to said read-out circuit;
in said read-out period, causes said read-out circuit to read out said signals; and
in said power-off period, ceases to supply power to said pixel array and said read-out circuit.

7. An image sensor comprising:

a pixel array, comprising a plurality of pixels, each pixel having a light receiving element;
a vertical scanning circuit, for serially activating rows of said pixel array to read out signals from pixels of an activated row;
sample and hold circuits, for sampling signals from the pixels of the activated row and holding them;
a horizontal scanning circuit, for serially activating said sample and hold circuits to read out a held signal from an activated sample and hold circuit onto a horizontal bus;
an amplifier circuit, for amplifying a signal on said horizontal bus or said signals read out from said pixels of said activated row; and
a control circuit, arranged to repeat a sequential operation of a light integration period, a read-out period and a power-off period,
wherein said control circuit:

in said light integration period, causes said pixel array to perform light integration for at least one frame period without supplying power to said sample and hold circuits and said horizontal scanning circuit;
in said read-out period, causes said vertical scanning circuit, said sample and hold circuits, and said horizontal scanning circuit to operate for one frame period; and
in said power-off period, ceases to supply power to said pixel array, said vertical scanning circuit, said sample and hold circuits, said horizontal scanning circuit and said amplifier circuit for at least one frame period.

8. An image sensor comprising:

a pixel array, comprising a plurality of pixels, each pixel having a light receiving element;
a read-out circuit, for scanning said pixel array to read out signals from pixels; and
a control circuit, arranged to repeat a sequential operation of a light integration period and a read-out period,
wherein said control circuit:

in said light integration period, causes said pixel array to perform light integration without supplying power to said read-out circuit; and
in said read-out period, causes said read-out circuit to read out said signals.

9. An image sensor comprising:

a pixel array, comprising a plurality of pixels, each pixel having a light receiving element;
a vertical scanning circuit, for serially activating rows of said pixel array to read out signals from pixels of an activated row;
sample and hold circuits, for sampling signals from the pixels of the activated row and holding

them;
a horizontal scanning circuit, for serially activating said sample and hold circuits to read out a held signal from an activated sample and hold circuit onto a horizontal bus;
an amplifier circuit, for amplifying the signal on said horizontal bus or said signals read out from said pixels of said activated row; and
a control circuit, for repeating a sequential operation of a light integration period and a read-out period,
wherein said control circuit:

in said light integration period, causes said pixel array to perform light integration for at least one frame period without supplying power to said sample and hold circuits and said horizontal scanning circuit; and
in said read-out period, causes said vertical scanning circuit, said sample and hold circuits, and said horizontal scanning circuit to operate for one frame period.

**10.** An image sensor comprising:

a pixel array, comprising a plurality of pixels, each pixel having a light receiving element;
a vertical scanning circuit, for serially activating rows of said pixel array to read out signals from pixels of an activated row;
sample and hold circuits, for sampling signals from the pixels of the activated row and holding them;
a horizontal scanning circuit, for serially activating said sample and hold circuits to read out a held signal from an activated sample and hold circuit onto a horizontal bus;
an amplifier circuit, for amplifying the signal on said horizontal bus or said signals read out from said pixels of said activated row; and
a control circuit, for repeating a sequential operation of a light integration period and a read-out period,
wherein said control circuit:

in said light integration period, causes said pixel array to perform light integration for one frame period without supplying power to said sample and hold circuits and said horizontal scanning circuit; and
in said read-out period, causes said vertical scanning circuit, said sample and hold circuits, and said horizontal scanning circuit to operate for at least one frame period.

FIG.1

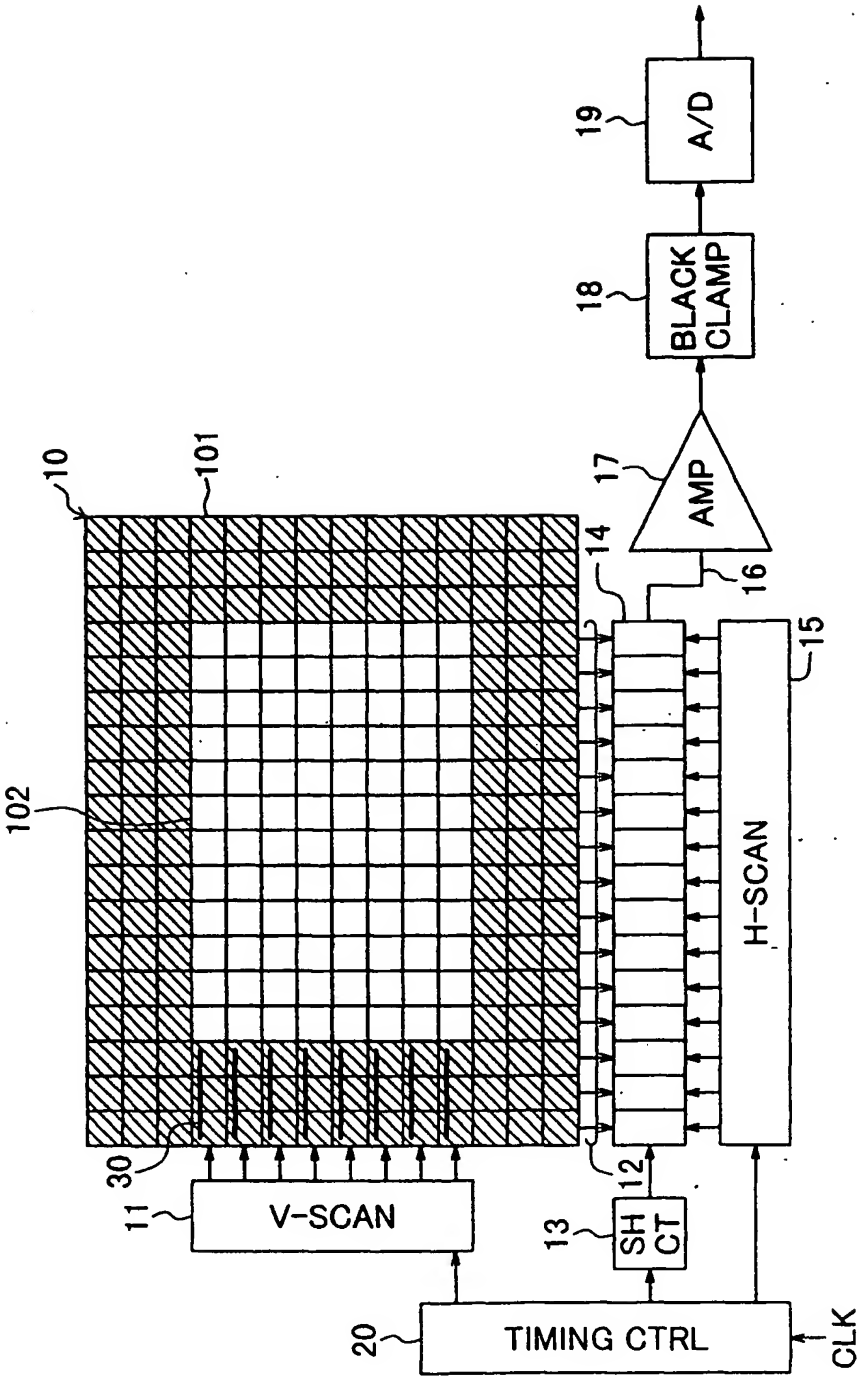
19
A/D
18
BLACK CLAMP
17
AMP
10
101
14
16
15
102
H-SCAN
30
12
11
V-SCAN
13
SH CT
20
TIMING CTRL
CLK

FIG.2

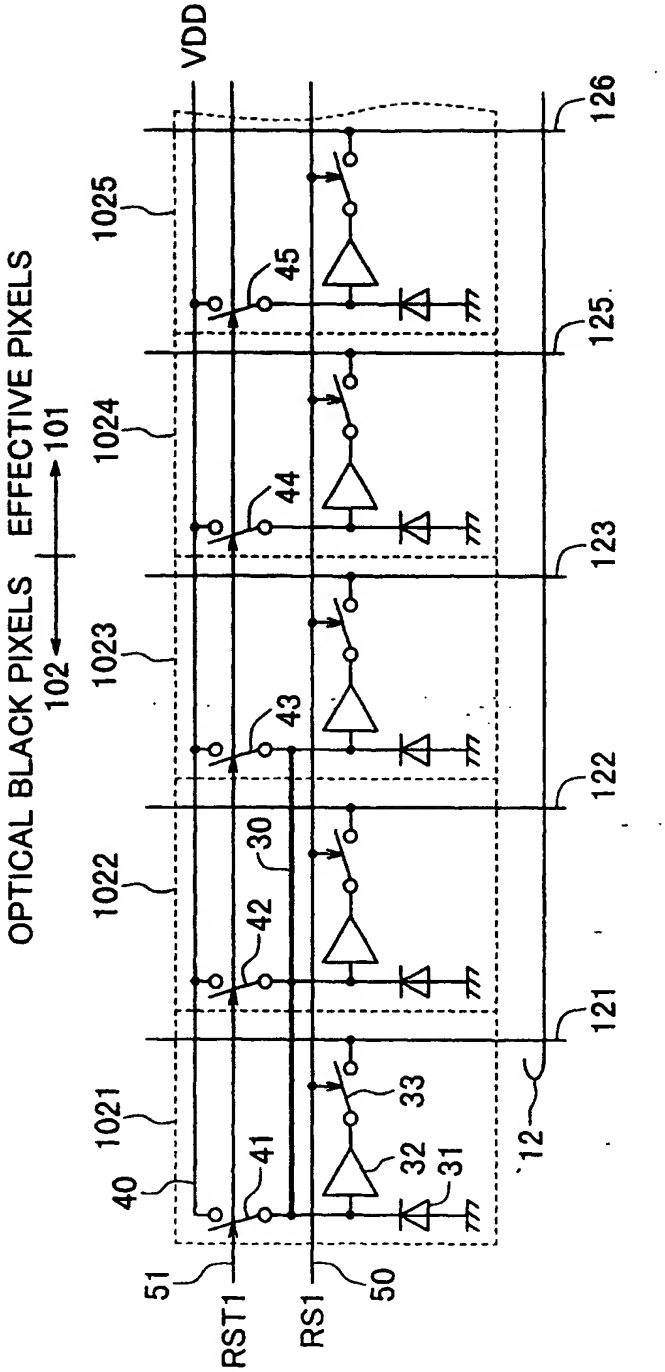
VDD
OPTICAL BLACK PIXELS
102
EFFECTIVE PIXELS
101
1021
1022
1023
1024
1025
126
125
123
122
121
12
40
41
42
43
44
45
30
31
32
33
51
50
RST1
RS1

FIG.3

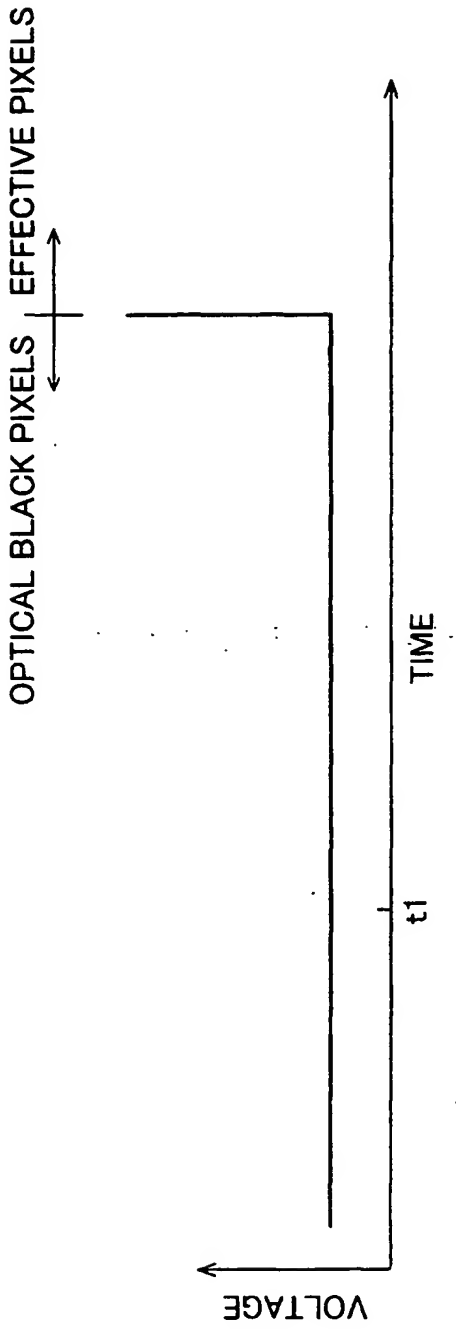

FIG.4

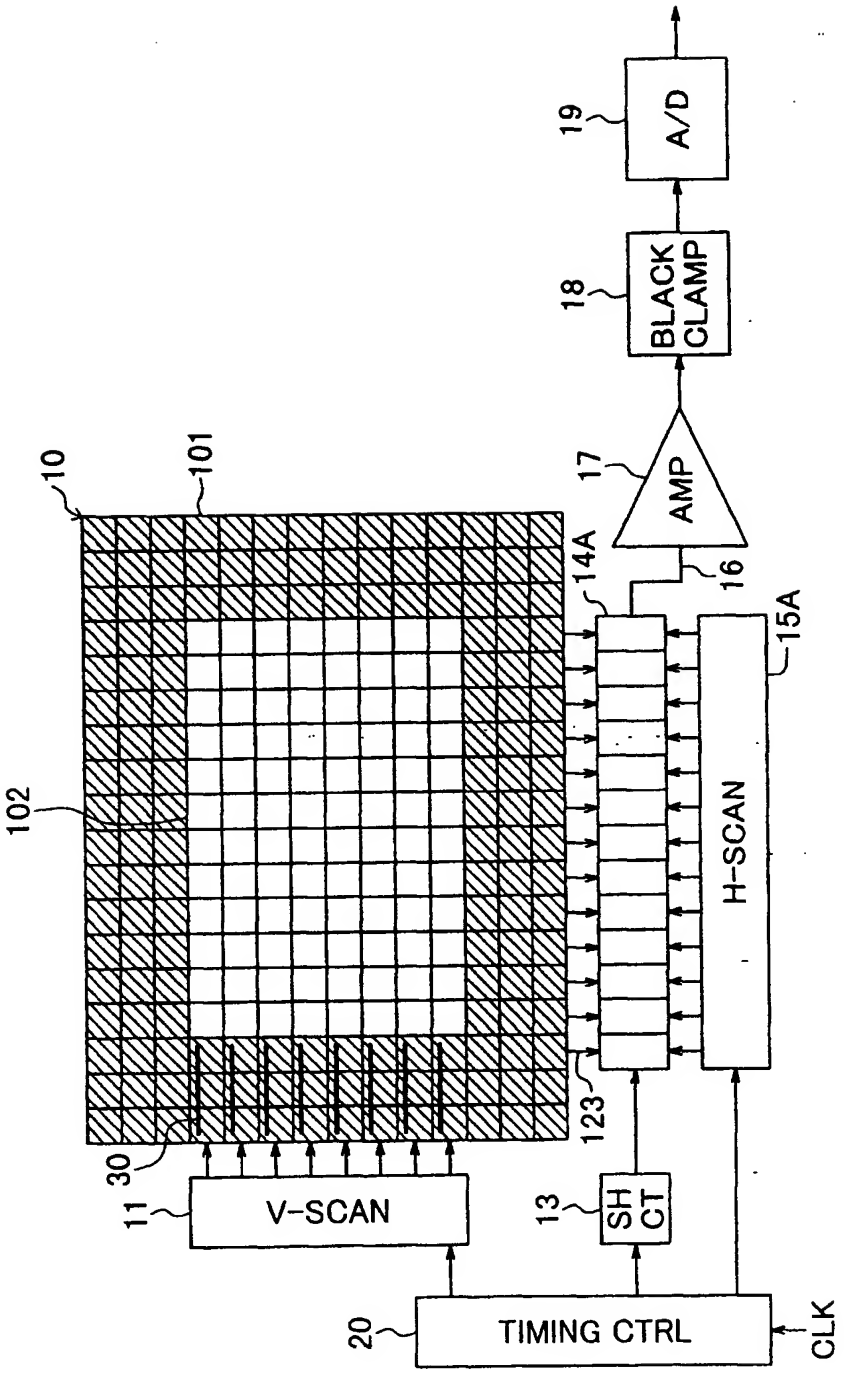
19
A/D
18
BLACK CLAMP
17
AMP
16
10
101
14A
15A
H-SCAN
102
123
30
11
V-SCAN
13
SH CT
20
TIMING CTRL
CLK

FIG.5

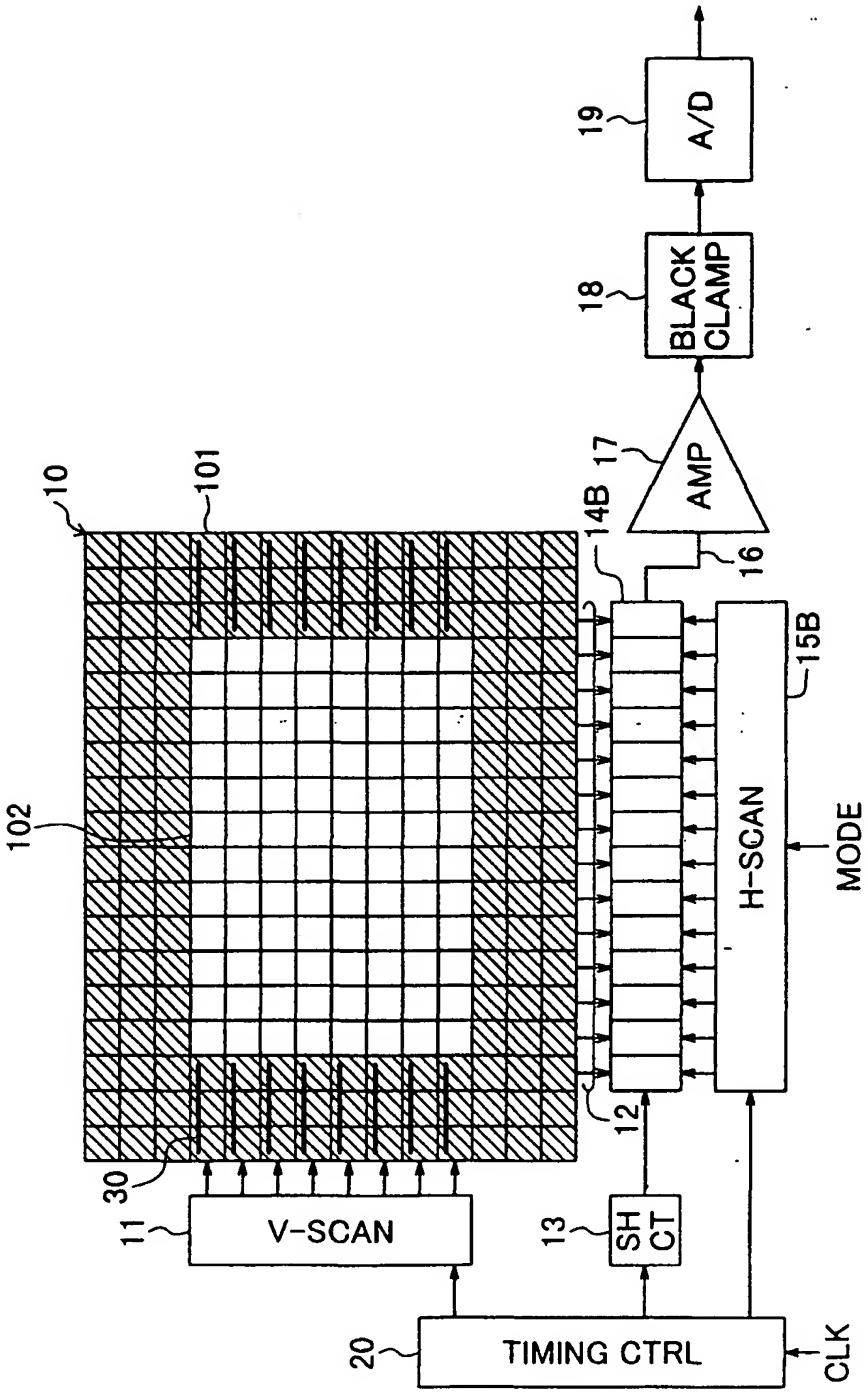
19
A/D
18
BLACK CLAMP
17
AMP
14B
16
10
101
102
15B
H-SCAN
MODE
12
30
11
V-SCAN
13
SH CT
20
TIMING CTRL
CLK

FIG.6

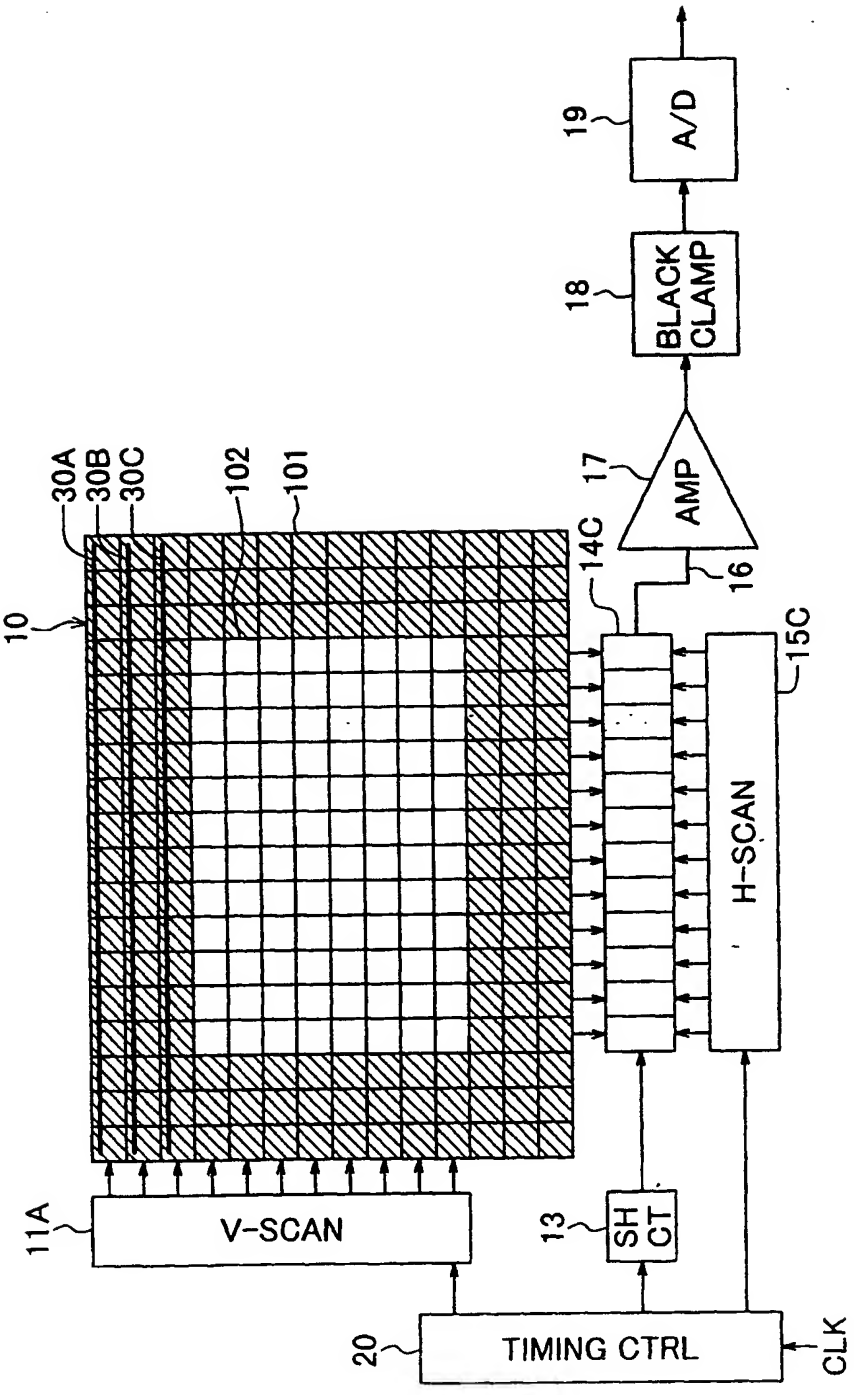
19
A/D
18
BLACK CLAMP
17
AMP
16
14C
15C
H-SCAN
30A
30B
30C
102
101
10
11A
V-SCAN
13
SH CT
20
TIMING CTRL
CLK

FIG.7

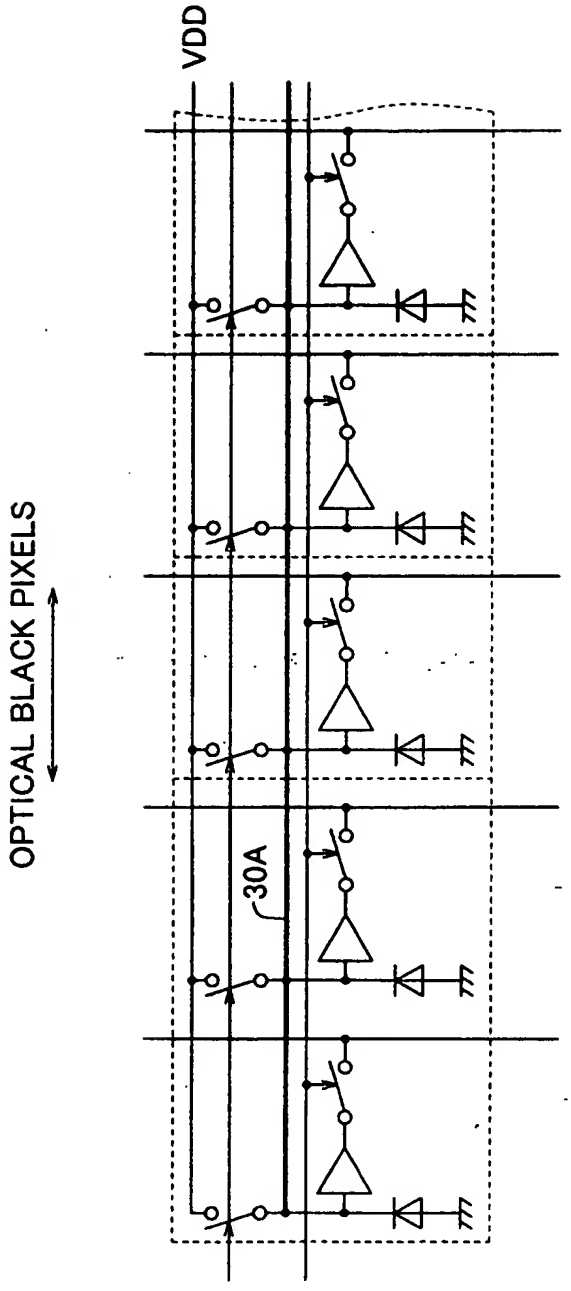

FIG.8

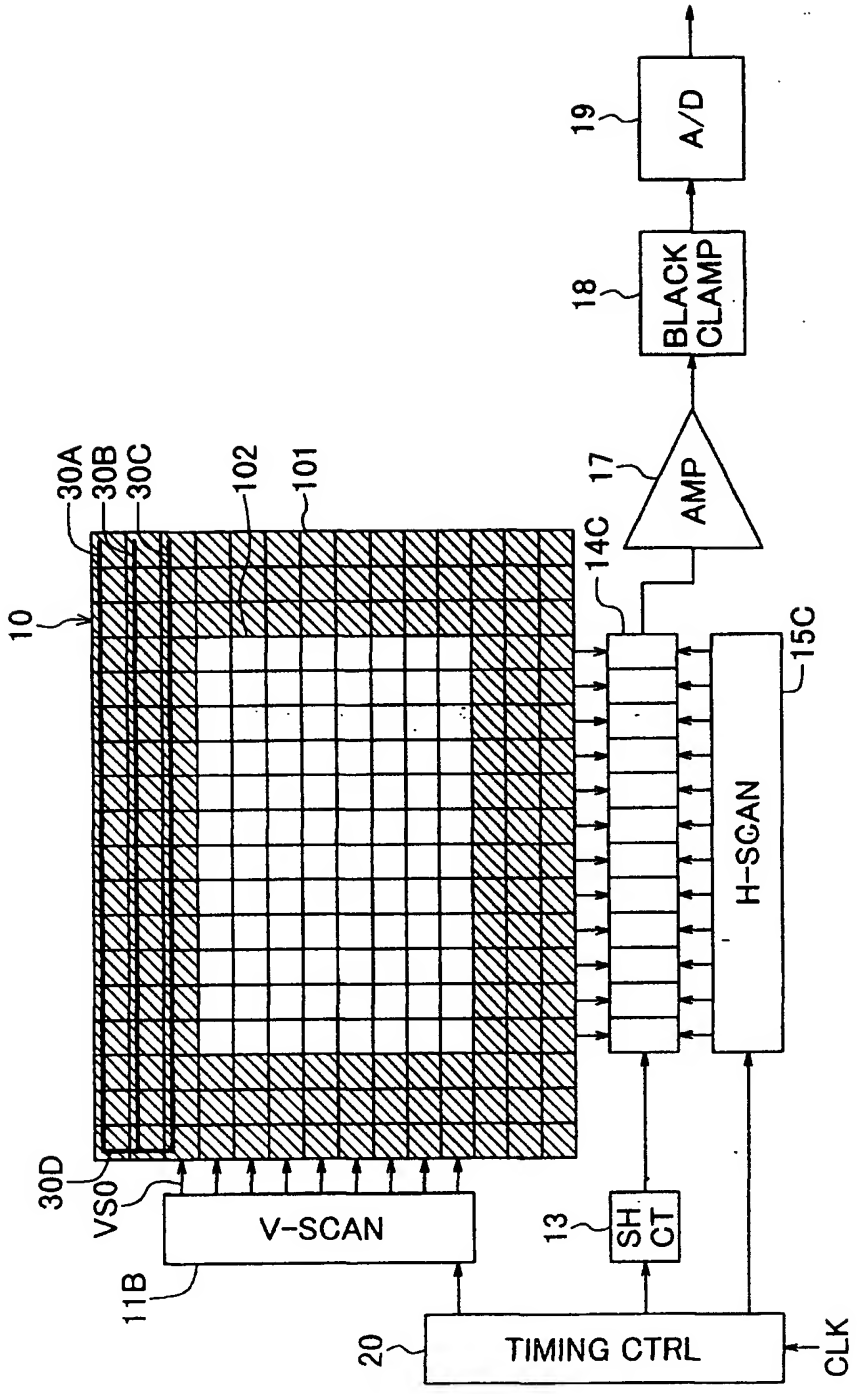
19
A/D
18
BLACK CLAMP
17
AMP
30A
30B
30C
102
101
14C
15C
10
H-SCAN
30D
VS0
V-SCAN
13
SH CT
11B
20
TIMING CTRL
CLK

FIG.9

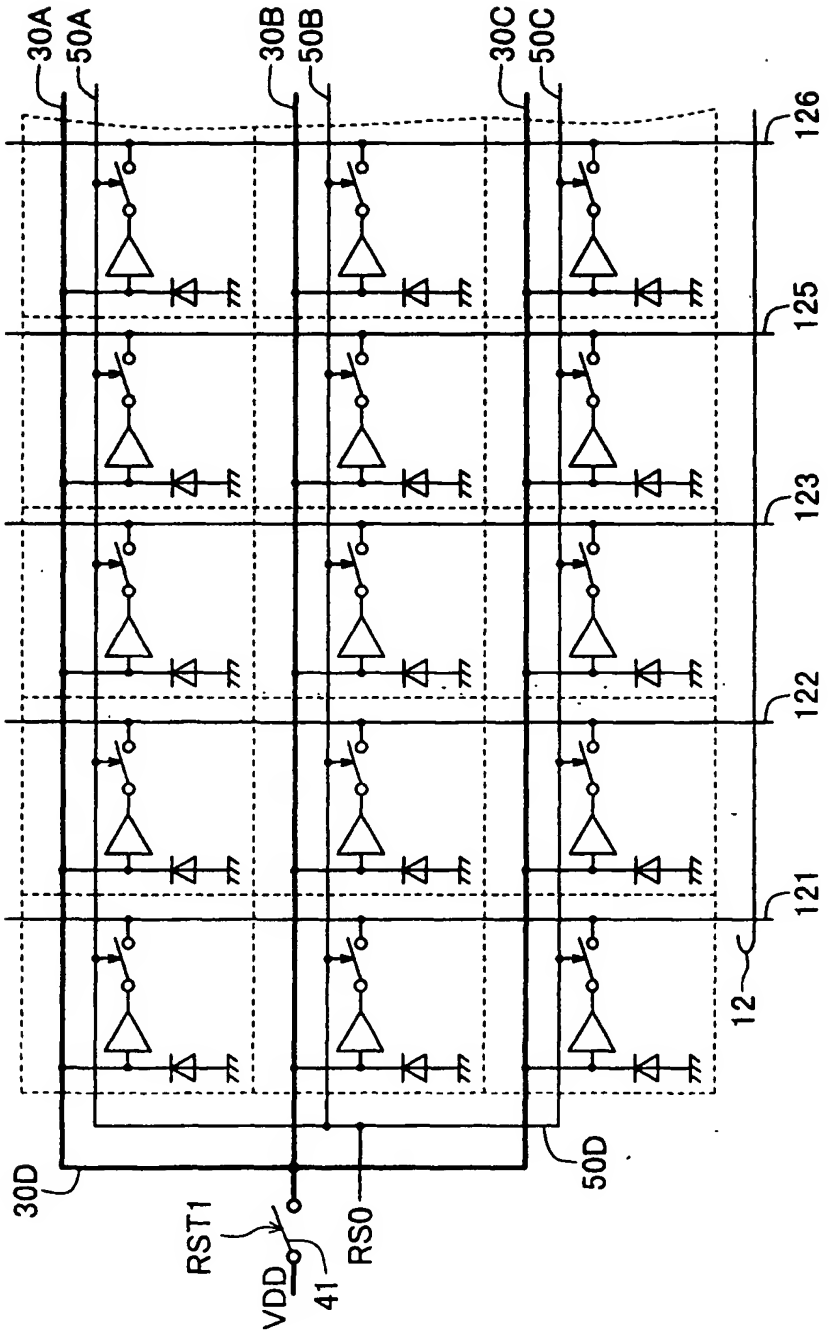
30A
50A
30B
50B
30C
50C
126
125
123
122
121
12
30D
50D
RST1
VDD
41
RS0

FIG.10

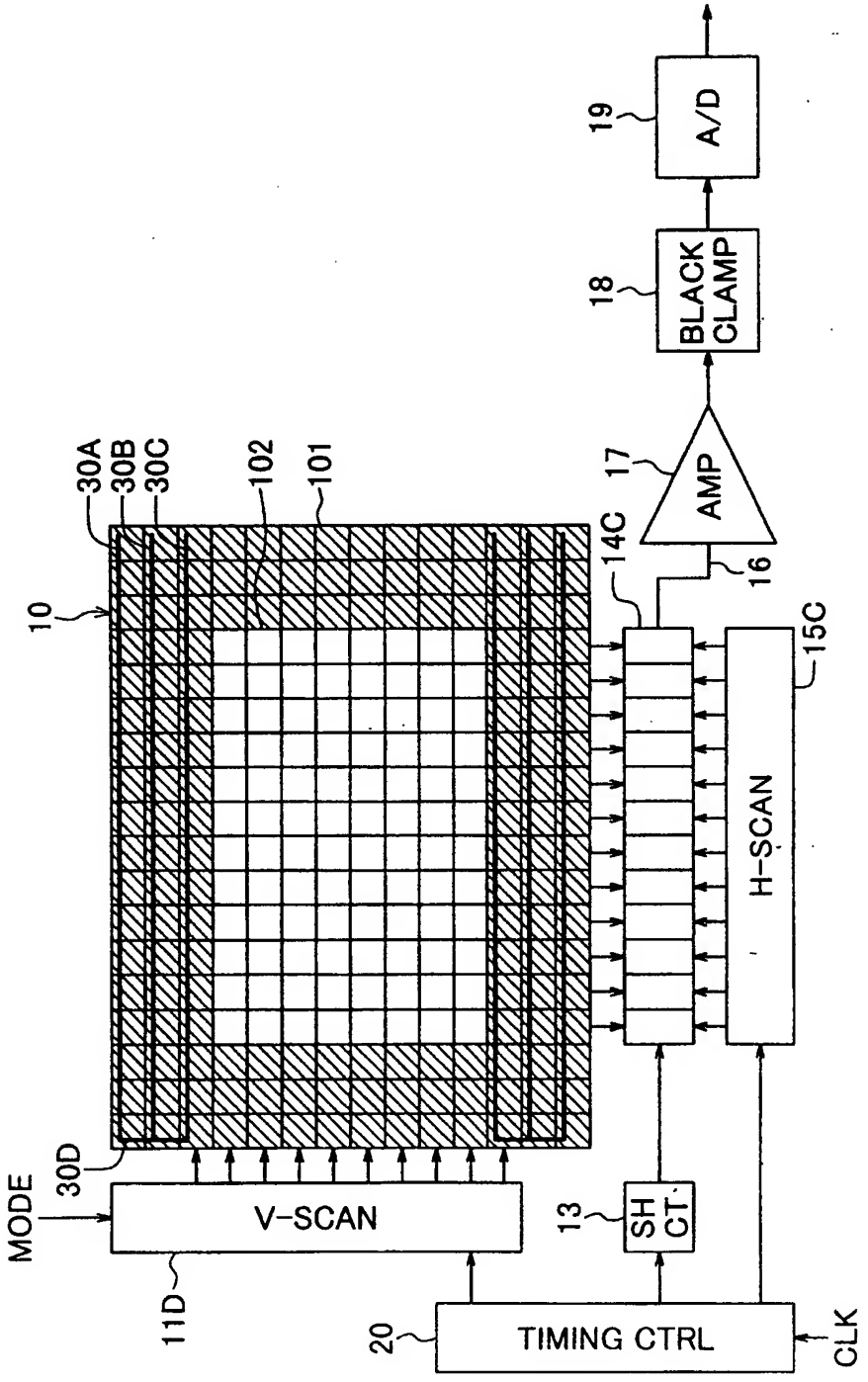
19
A/D
18
BLACK CLAMP
17
AMP
16
14C
15C
H-SCAN
30A
30B
30C
102
101
10
30D
MODE
V-SCAN
11D
13
SH CT
20
TIMING CTRL
CLK

FIG.11

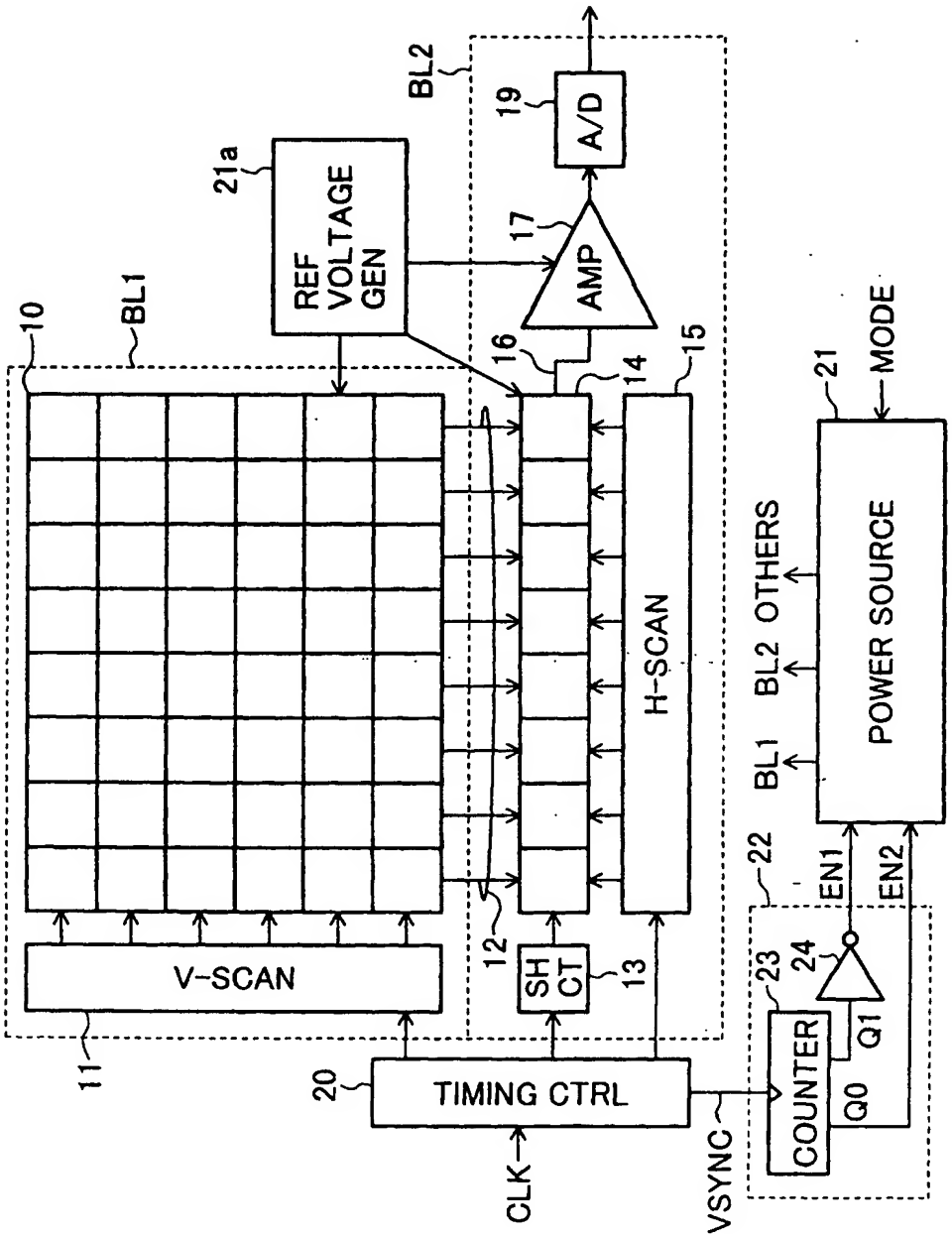
10
BL1
BL2
19
A/D
21a
REF VOLTAGE GEN
17
AMP
16
14
15
21
MODE
POWER SOURCE
BL2 OTHERS
BL1
H-SCAN
V-SCAN
12
SH CT
13
11
20
TIMING CTRL
CLK
VSYNC
22
EN1
EN2
23
24
COUNTER
Q1
Q0

FIG.12

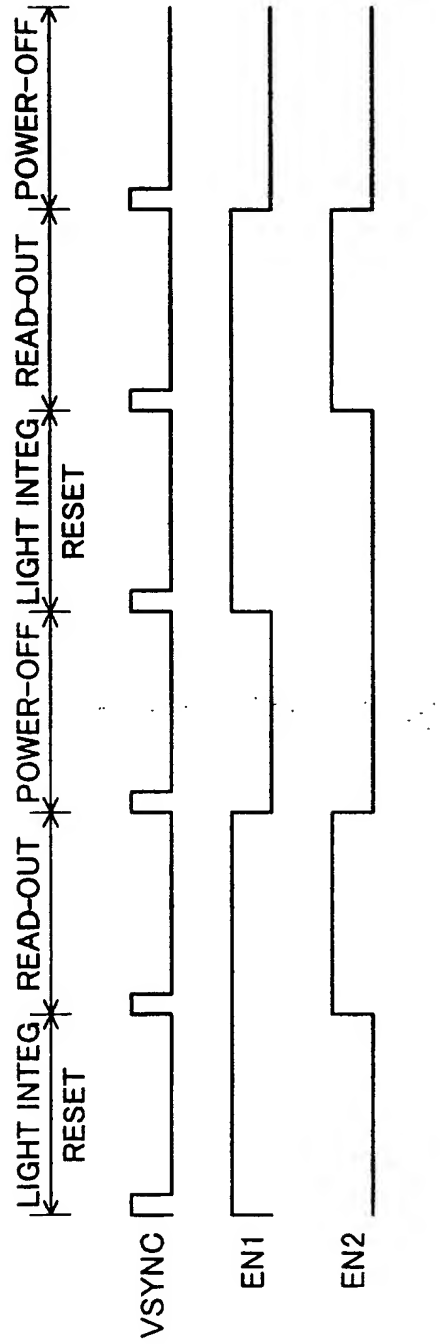
LIGHT INTEG
RESET
READ-OUT
POWER-OFF
LIGHT INTEG
RESET
READ-OUT
POWER-OFF
VSYNC
EN1
EN2

FIG.13

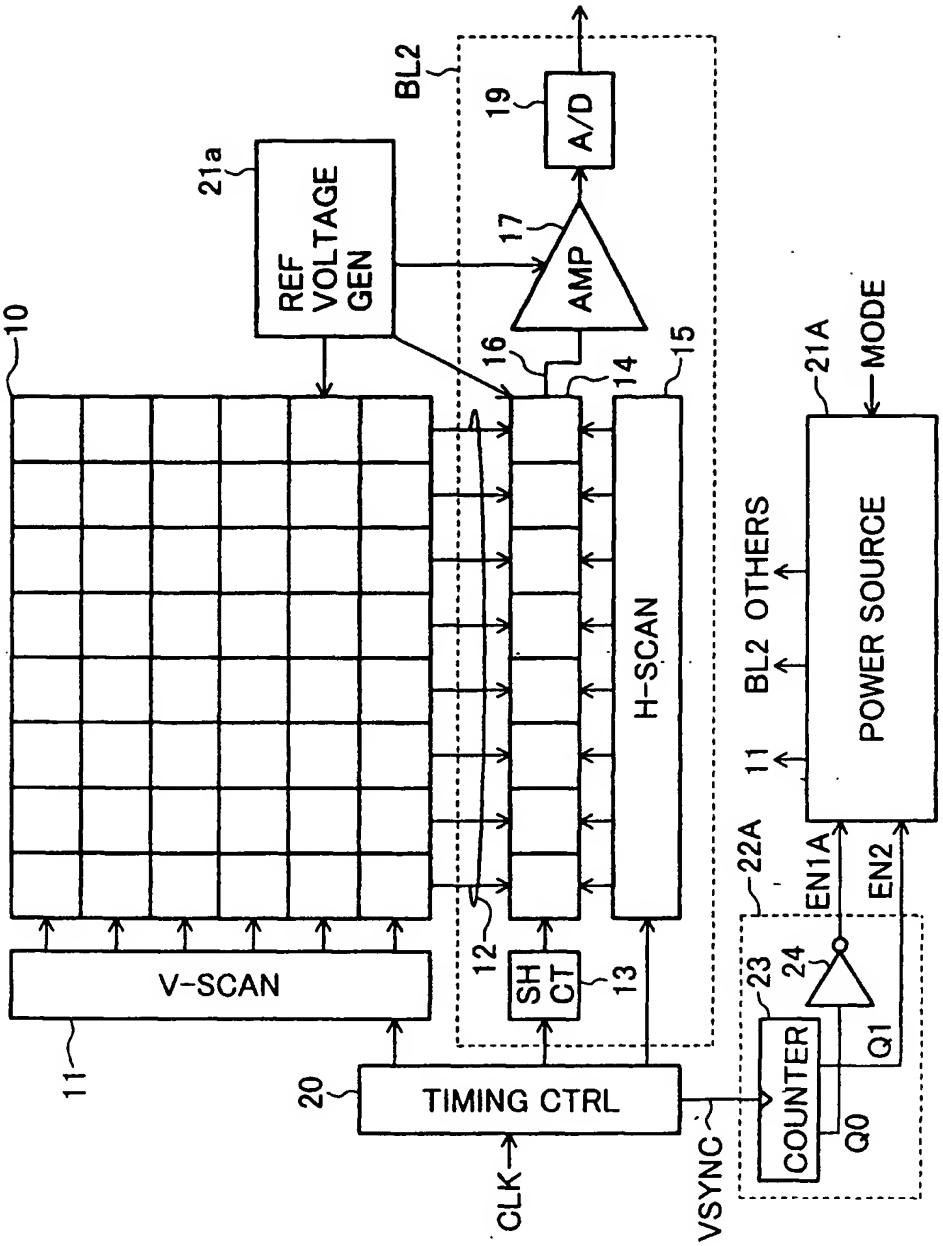
10
11
12
13
14
15
16
17
19
20
21a
21A
22A
23
24
BL2
REF VOLTAGE GEN
A/D
AMP
V-SCAN
SH CT
H-SCAN
TIMING CTRL
CLK
VSYNC
COUNTER
Q0
Q1
EN1A
EN2
BL2 OTHERS
POWER SOURCE
MODE

FIG.14

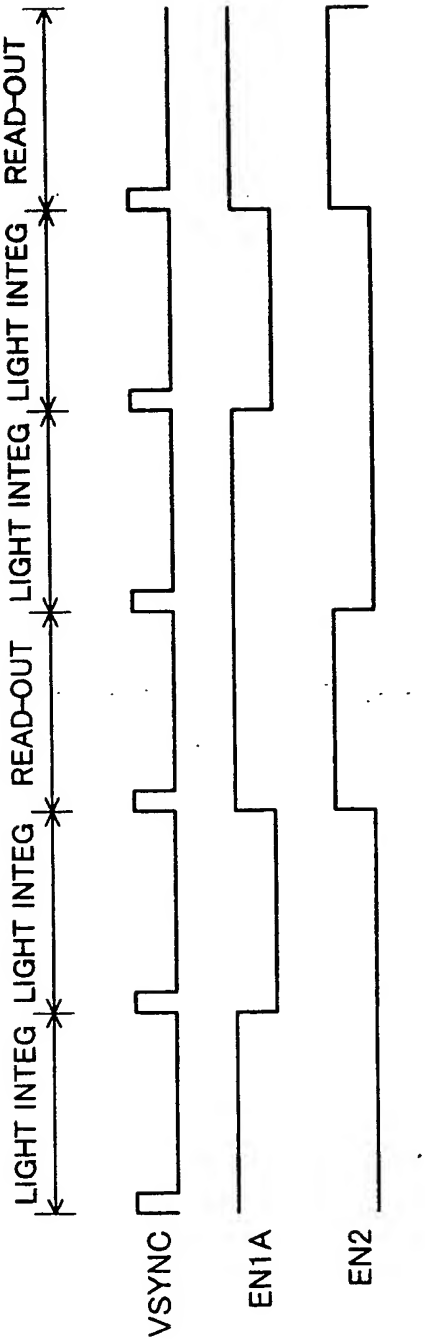
LIGHT INTEG
LIGHT INTEG
READ-OUT
LIGHT INTEG
LIGHT INTEG
READ-OUT
VSYNC
EN1A
EN2

FIG.15

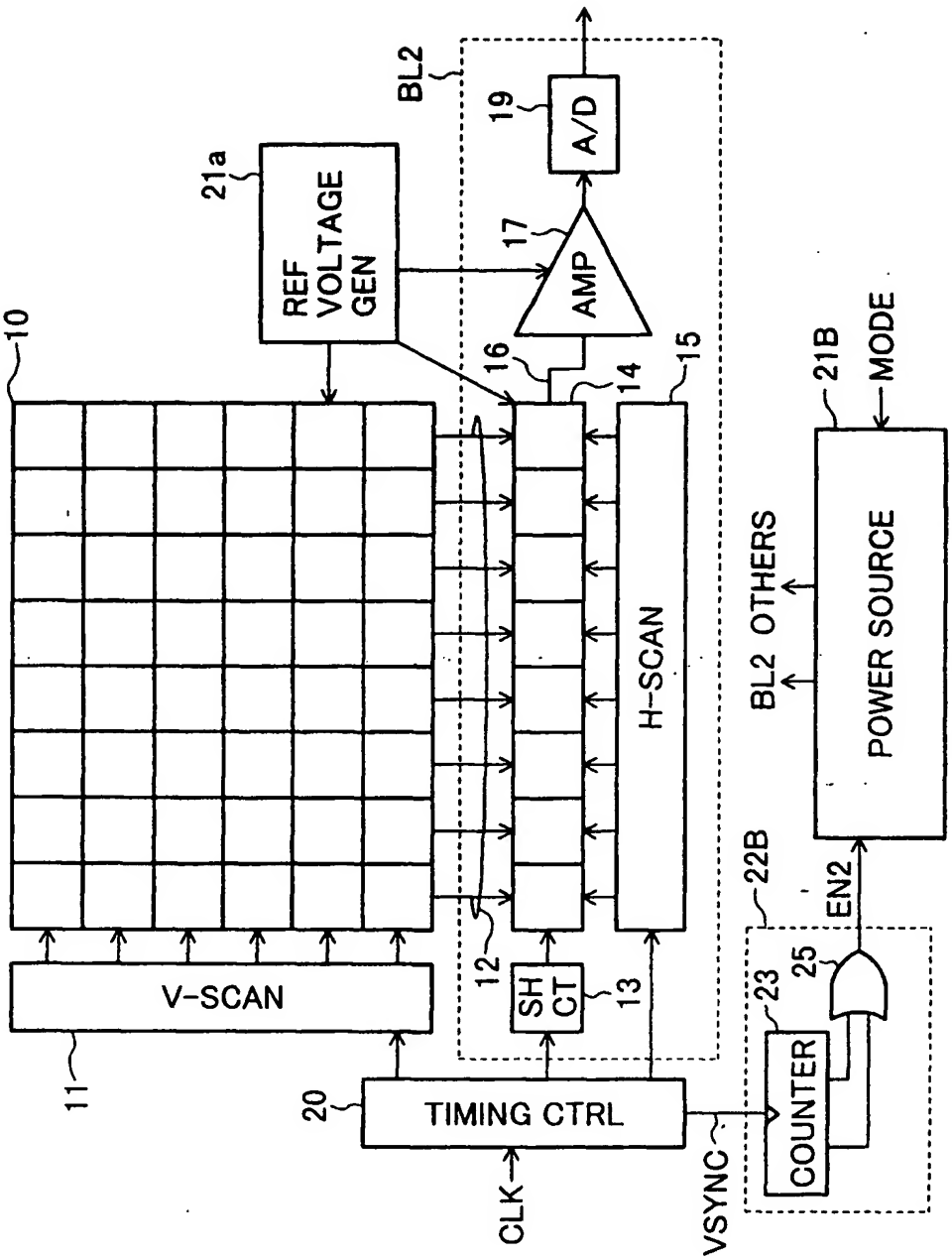
BL2
19
A/D
21a
REF VOLTAGE GEN
17
AMP
10
16
14
15
21B
MODE
BL2 OTHERS
POWER SOURCE
H-SCAN
22B
EN2
12
SH CT
13
25
23
V-SCAN
11
20
TIMING CTRL
COUNTER
CLK
VSYNC

FIG.16

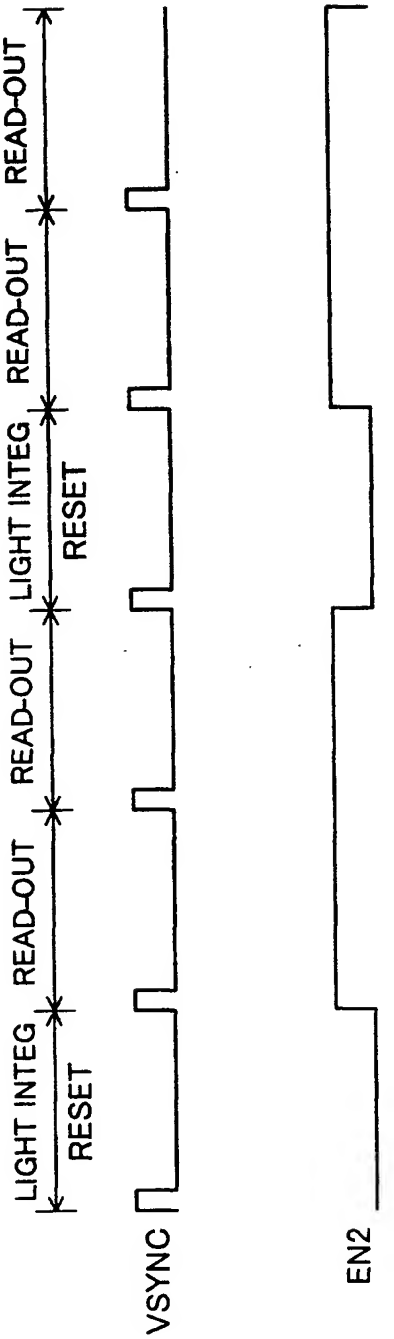
LIGHT INTEG
RESET
READ-OUT
READ-OUT
LIGHT INTEG
RESET
READ-OUT
VSYNC
EN2

FIG.17

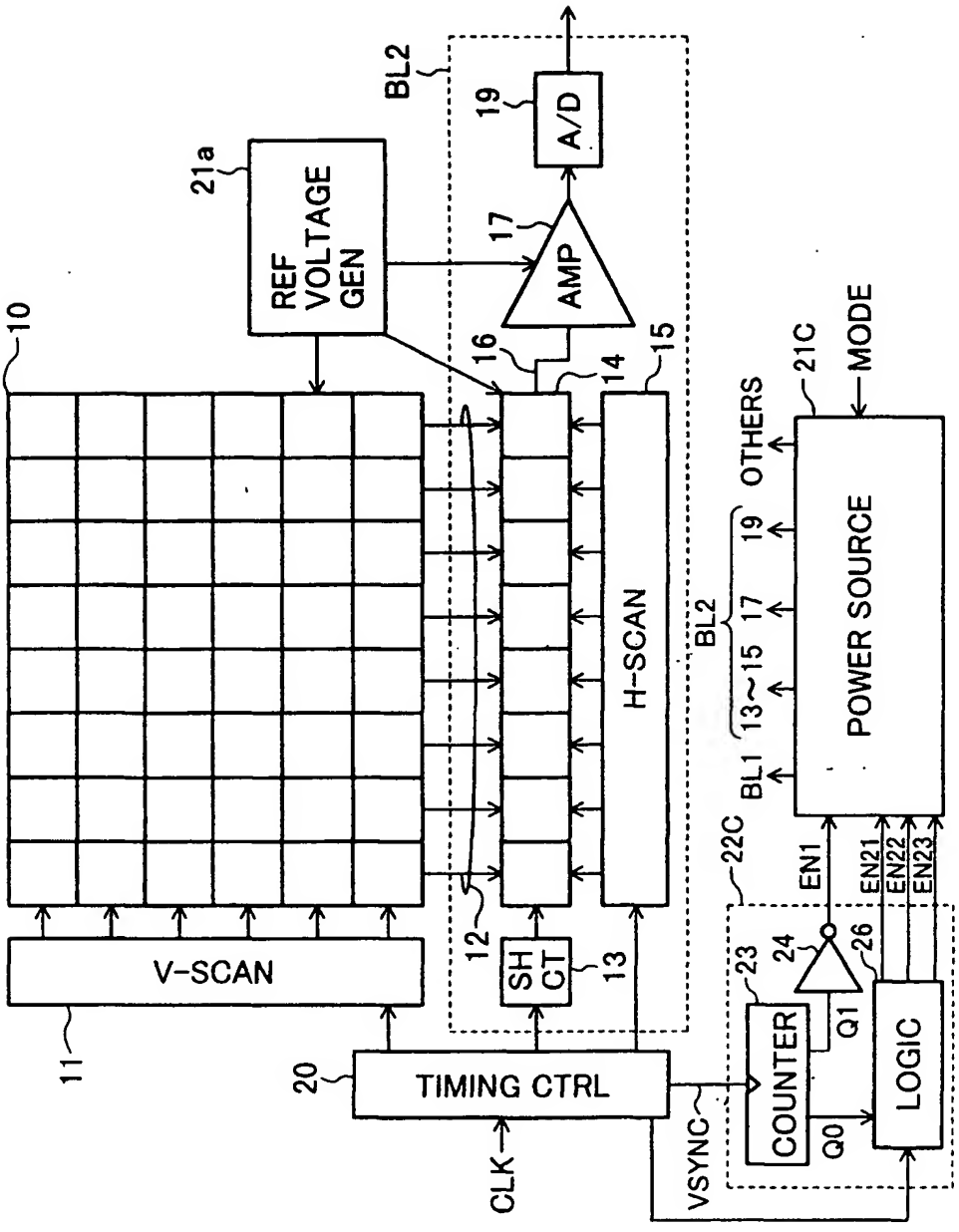
BL2
19
A/D
21a
REF VOLTAGE GEN
17
AMP
10
16
14
15
H-SCAN
V-SCAN
12
SH CT
13
11
20
TIMING CTRL
CLK
VSYNC
BL2
BL1
13~15
17
19
OTHERS
21C
MODE
POWER SOURCE
22C
EN1
EN21
EN22
EN23
23
24
26
Q1
Q0
COUNTER
LOGIC

FIG.18

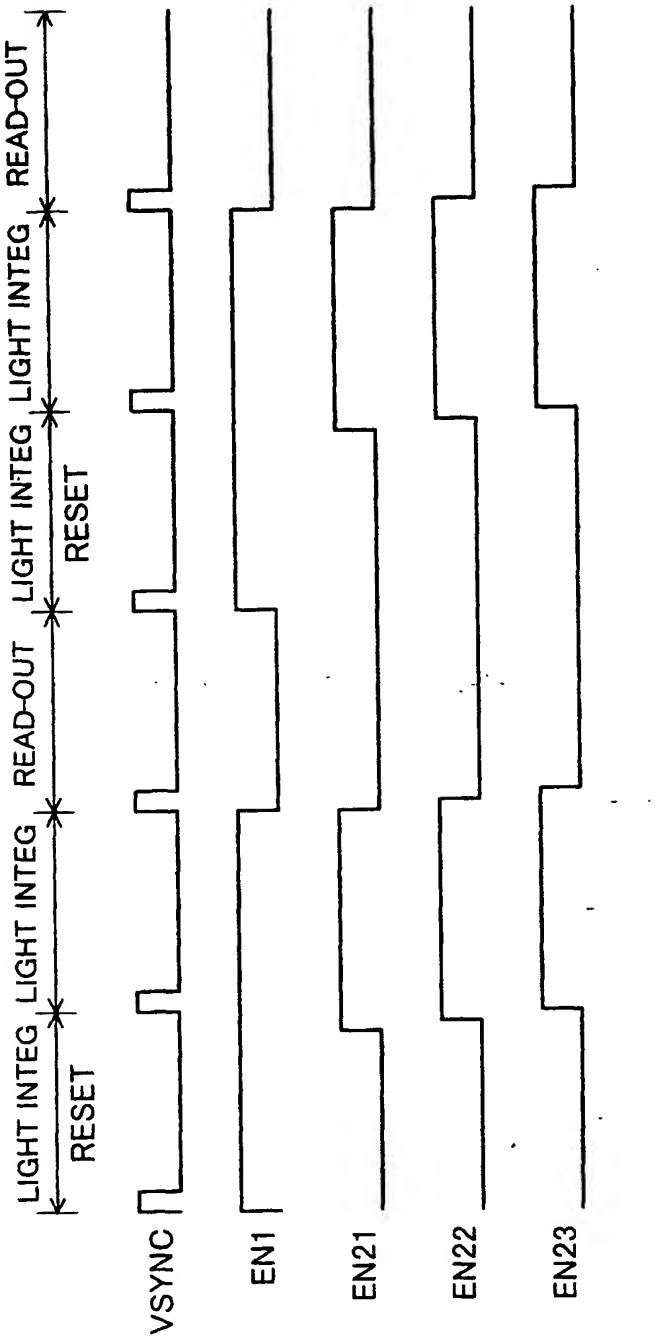
LIGHT INTEG
RESET
LIGHT INTEG
READ-OUT
LIGHT INTEG
RESET
LIGHT INTEG
READ-OUT
VSYNC
EN1
EN21
EN22
EN23

FIG.19
prior art